VQ2004J

P-Channel Enhancement-Mode MOS Transistor

Product Summary

$V_{(BR)DSS}$ Min (V)	$r_{DS(on)}$ Max (Ω)	$V_{GS(th)}$ (V)	I_D (A)
–60	5 @ V_{GS} = –10 V	–2 to –4.5	–0.41

Features

- High-Side Switching
- Low On-Resistance: 2.5 Ω
- Moderate Threshold: –3.4 V
- Fast Switching Speed: 40 ns
- Low Input Capacitance: 75 pF

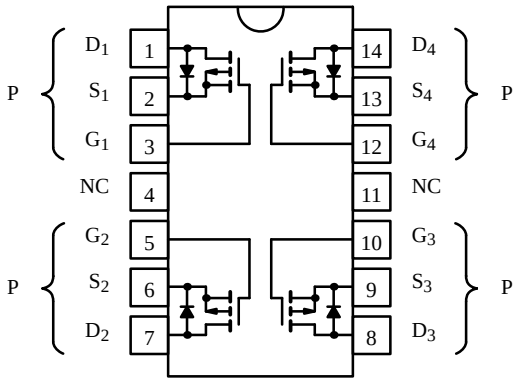
Benefits

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Switching
- Easily Driven Without Buffer

Applications

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Power Supply, Converter Circuits
- Motor Control

Dual-In-Line



Top View

Plastic: VQ2004J

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Single	Total Quad	Unit
Drain-Source Voltage		V_{DS}	–60		V
Gate-Source Voltage		V_{GS}	± 30		
Continuous Drain Current (T_J = 150°C)	T_A= 25°C	I_D	–0.41		A
	T_A= 100°C		–0.23		
Pulsed Drain Current[a]		I_{DM}	–3		
Power Dissipation	T_A= 25°C	P_D	1.3	2	W
	T_A= 100°C		0.52	0.8	
Maximum Junction-to-Ambient		R_{thJA}	96	62.5	°C/W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Notes
a. Pulse width limited by maximum junction temperature.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70220.

Specifications[a]

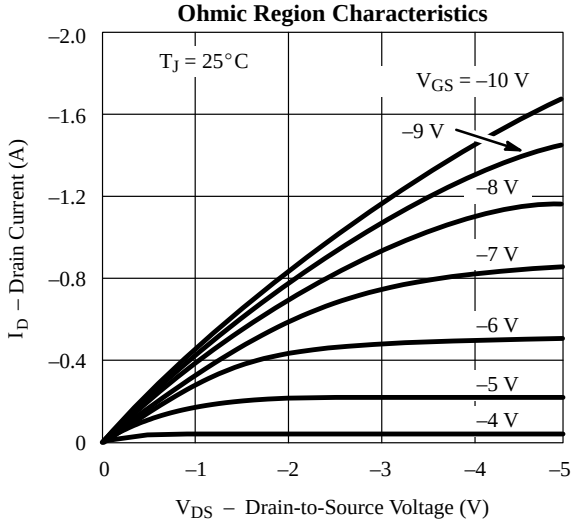
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ[b]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = –10 µA	–60	–110		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –1 mA	–2	–3.4	–4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V			±100	nA
		T_J = 125°C			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–10	µA
		V_{DS} = –48 V, V_{GS} = 0 V, T_J = 125°C			–500	µA
On-State Drain Current[c]	$I_{D(on)}$	V_{DS} = –10 V, V_{GS} = –10 V	–1	–2		A
Drain-Source On-Resistance[c]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –1 A		2.5	5	Ω
		T_J = 125°C		4.4	8	Ω
Forward Transconductance[c]	g_{fs}	V_{DS} = –10 V, I_D = –0.5 A	200	325		mS
Common Source Output Conductance[c]	g_{os}	V_{DS} = –7.5 V, I_D = –0.1 A		0.45		mS
Dynamic						
Input Capacitance	C_{iss}	V_{DS} = –25 V, V_{GS} = 0 V f = 1 MHz		75	150	pF
Output Capacitance	C_{oss}			40	60	pF
Reverse Transfer Capacitance	C_{rss}			18	25	pF
Switching[d]						
Turn-On Time	$t_{d(on)}$	V_{DD} = –25 V, R_L = 47 Ω I_D ≅ –0.5 A, V_{GEN} = –10 V R_G = 25 Ω		11	15	ns
	t_r			30	40	ns
Turn-Off Time	$t_{d(off)}$			20	30	ns
	t_f			20	30	ns

Notes
a. T_A = 25°C unless otherwise noted.
b. For DESIGN AID ONLY, not subject to production testing.
c. Pulse test: PW ≤300 µs duty cycle ≤2%.
d. Switching time is essentially independent of operating temperature.

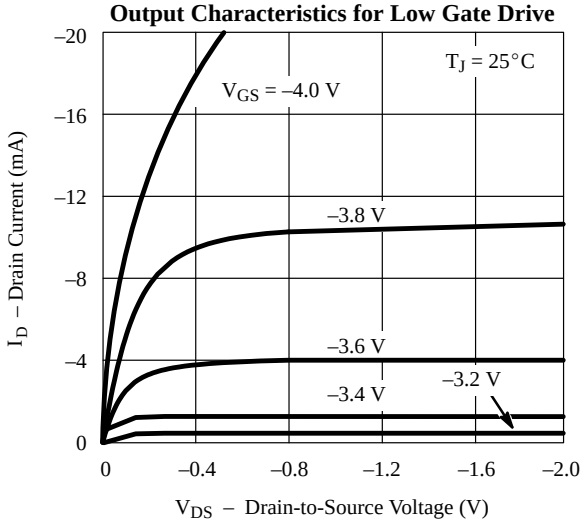
VPDV10

Typical Characteristics (25°C Unless Otherwise Noted)

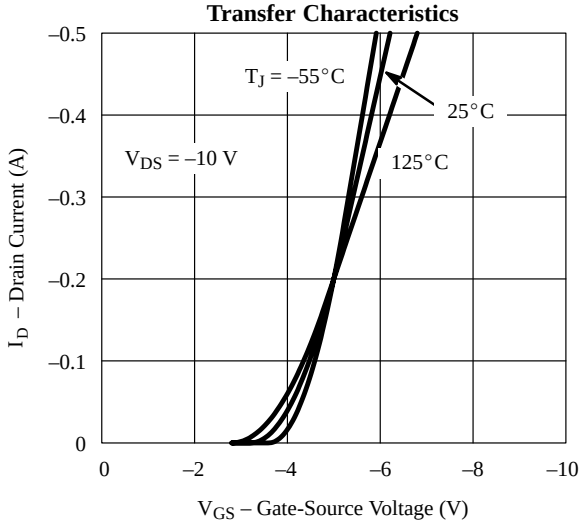
Ohmic Region Characteristics



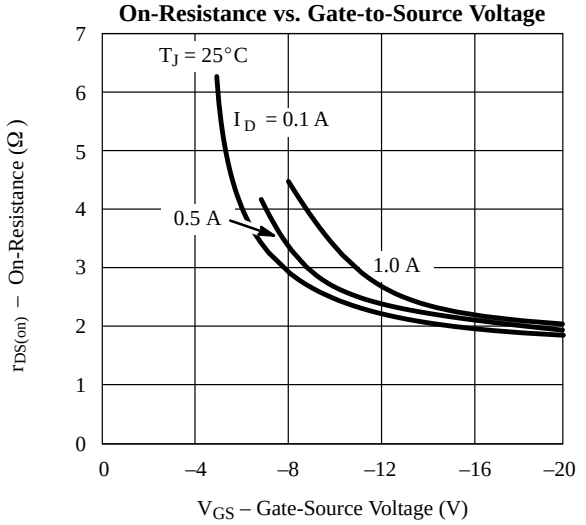
Output Characteristics for Low Gate Drive



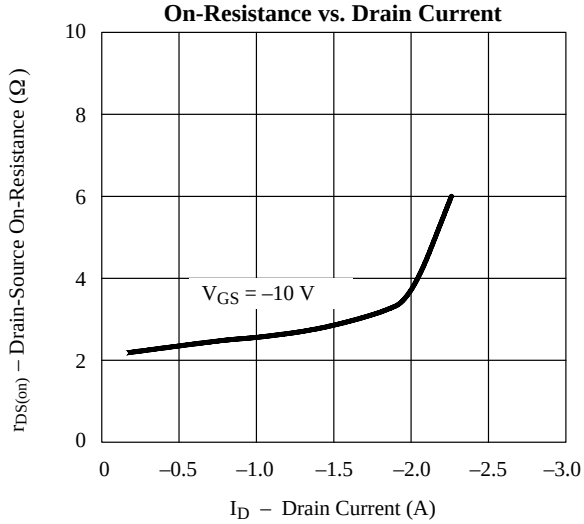
Transfer Characteristics



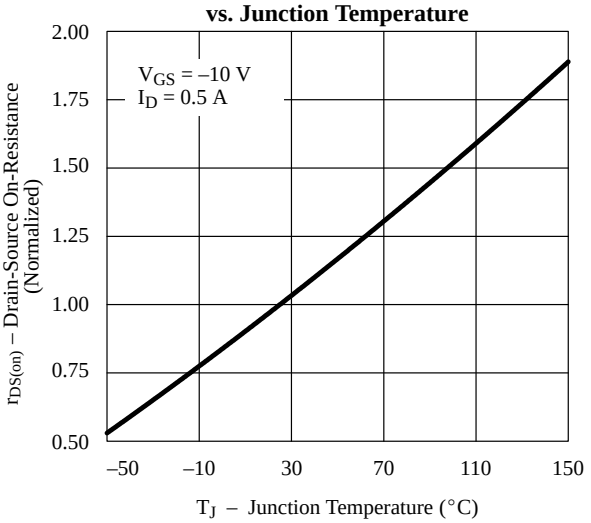
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Drain Current

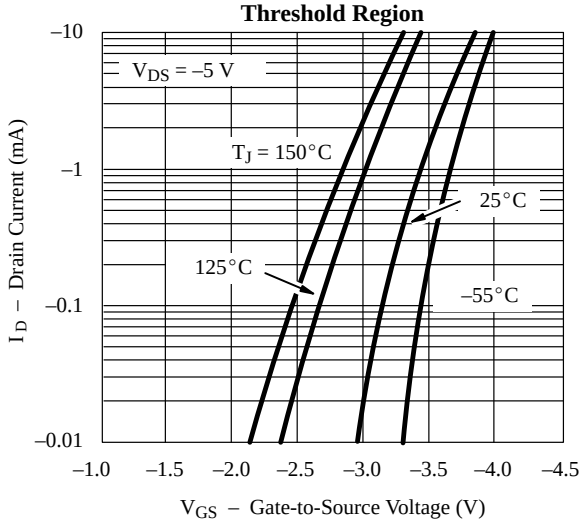


Normalized On-Resistance vs. Junction Temperature

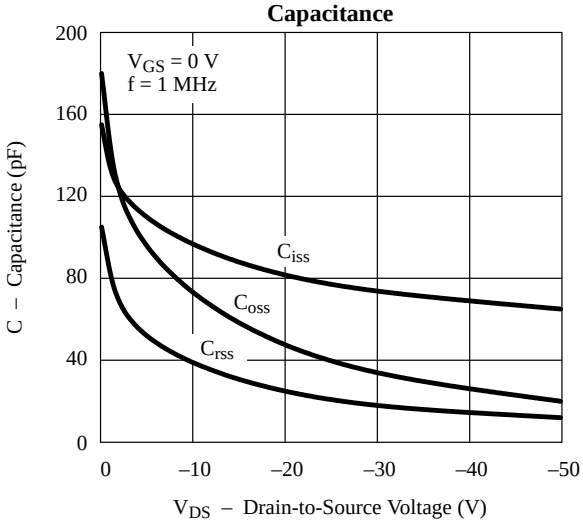


Typical Characteristics (25°C Unless Otherwise Noted) (Cont'd)

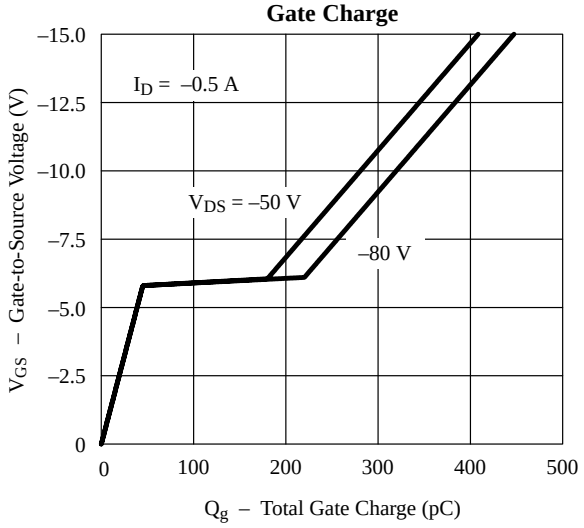
Threshold Region



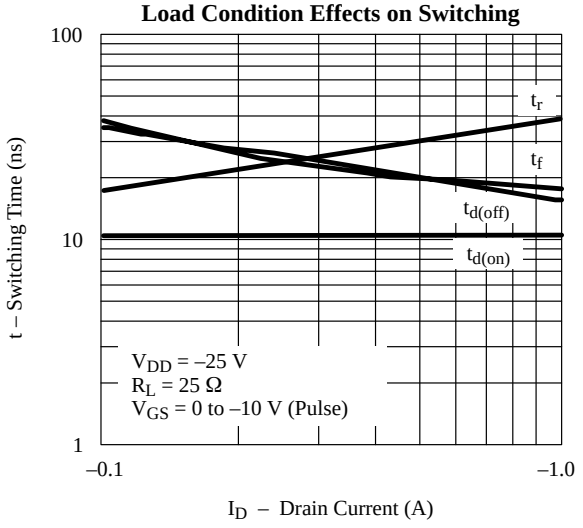
Capacitance



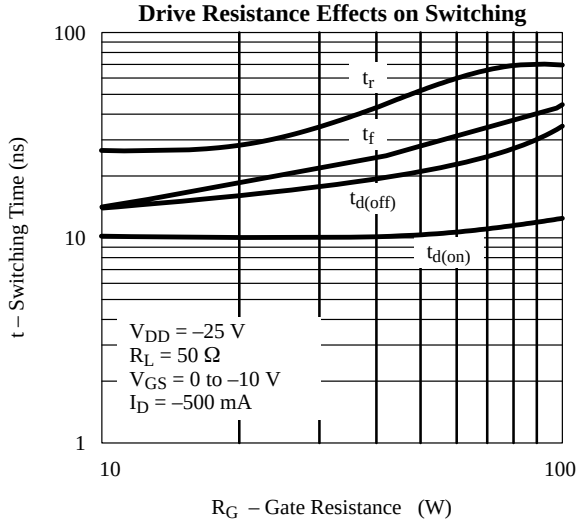
Gate Charge



Load Condition Effects on Switching



Drive Resistance Effects on Switching



Transconductance